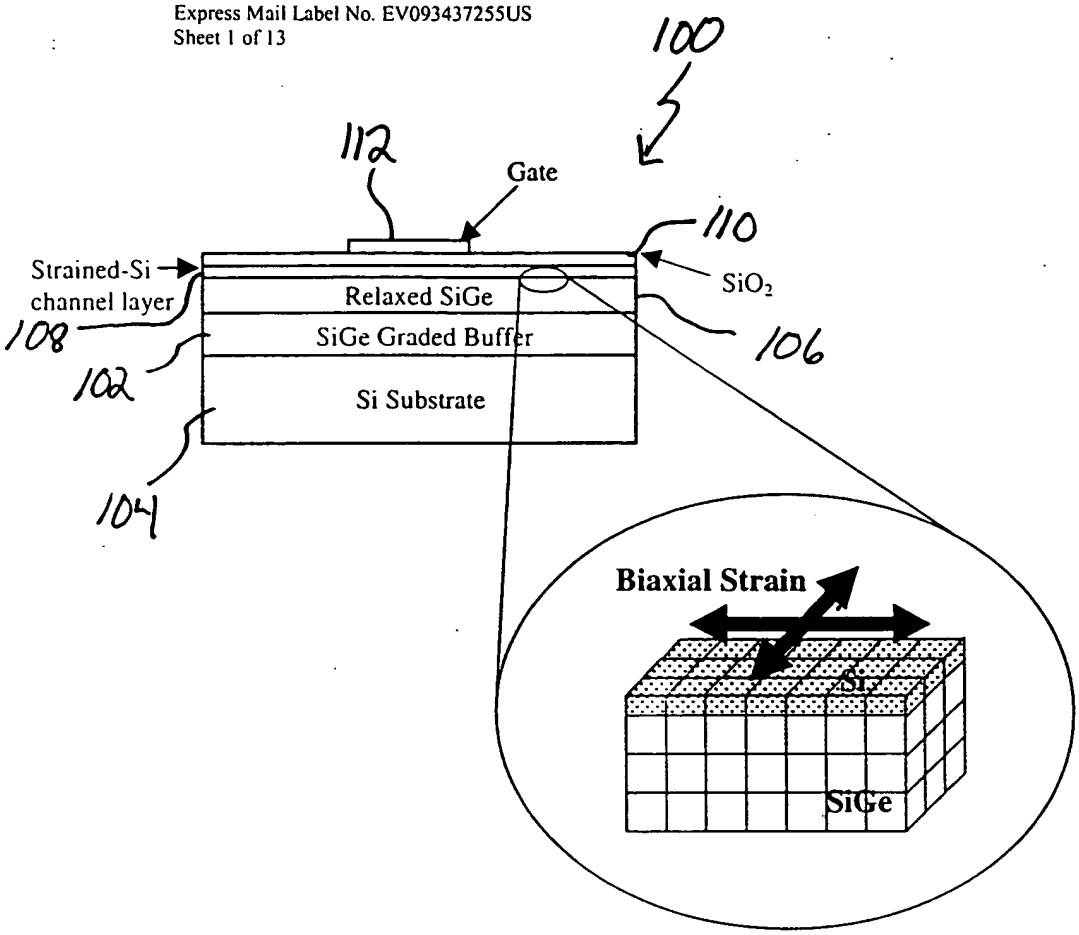

100
112
Gate
110
Strained-Si
channel layer
108
SiO_2
Relaxed SiGe
106
SiGe Graded Buffer
102
Si Substrate
104
Biaxial Strain
Si
SiGe

Fig. 1

Fig. 2A

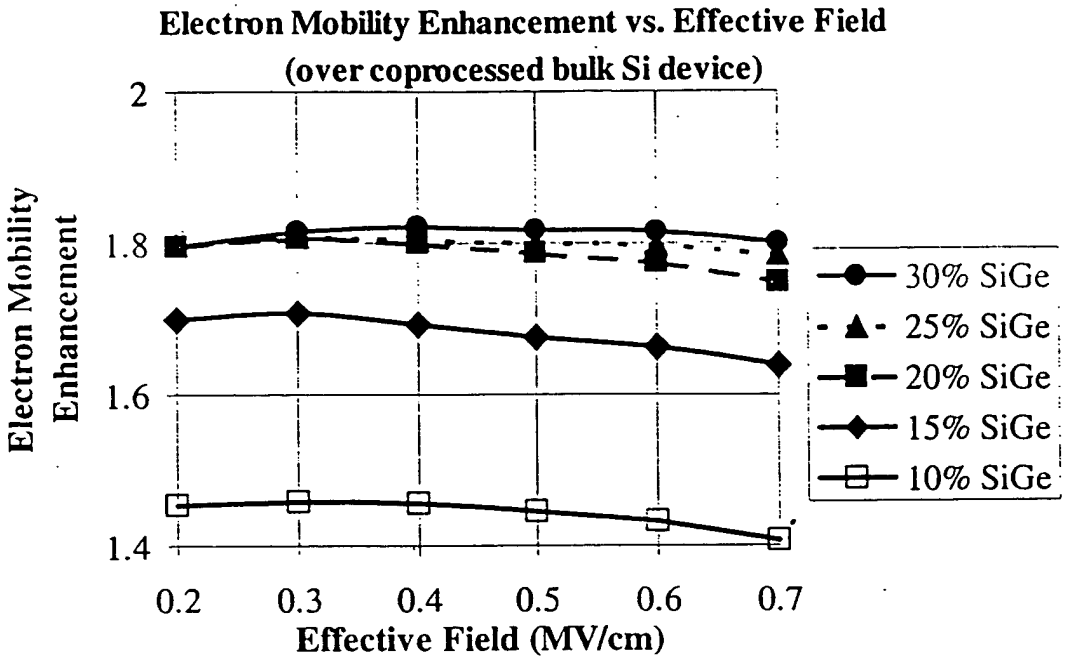
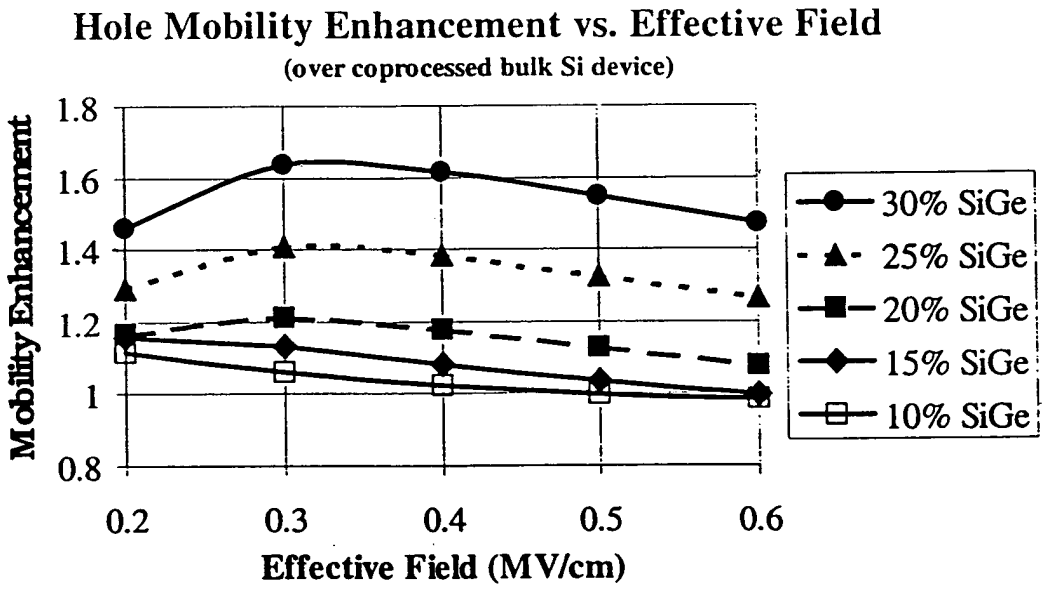

Electron Mobility Enhancement vs. Effective Field
(over coprocessed bulk Si device)
Electron Mobility Enhancement
2
1.8
1.6
1.4
0.2
0.3
0.4
0.5
0.6
0.7
Effective Field (MV/cm)
30% SiGe
25% SiGe
20% SiGe
15% SiGe
10% SiGe

Fig. 2B


Hole Mobility Enhancement vs. Effective Field
(over coprocessed bulk Si device)
Mobility Enhancement
1.8
1.6
1.4
1.2
1
0.8
0.2
0.3
0.4
0.5
0.6
Effective Field (MV/cm)
30% SiGe
25% SiGe
20% SiGe
15% SiGe
10% SiGe

Type of Surface	Average Roughness (nm)
As-grown graded composition relaxed SiGe	7.9
Planarized SiGe	0.57
Regrowth SiGe	~0.6

Fig. 3

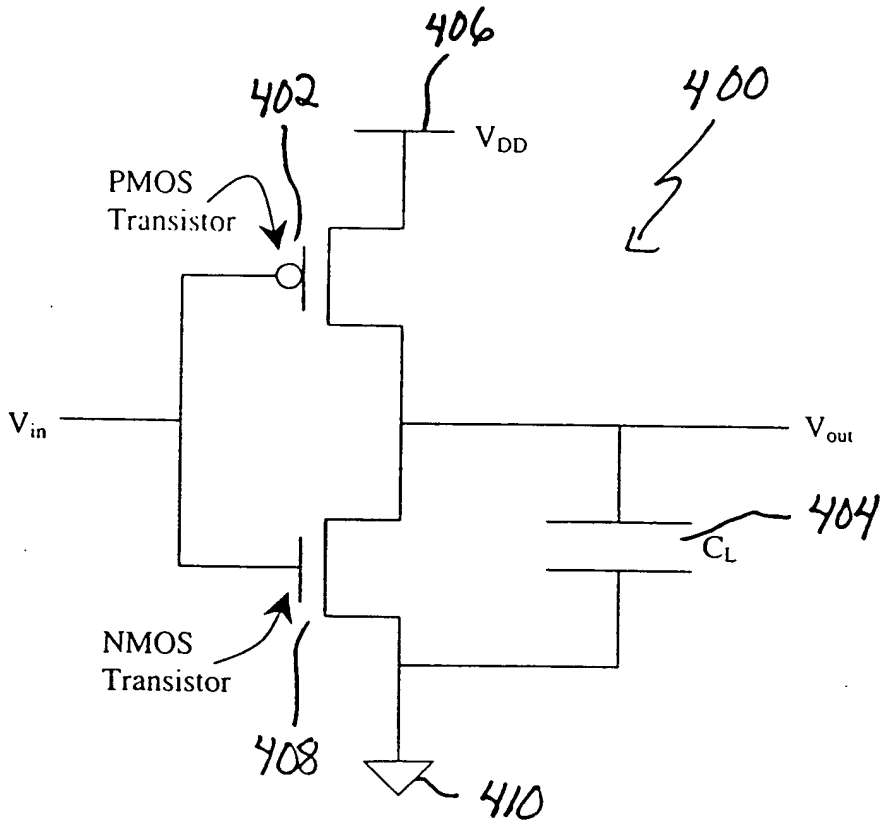

406
402
400
V_{DD}
PMOS
Transistor
V_{in}
V_{out}
404
C_L
NMOS
Transistor
408
410

Fig. 4

Fig. 5A

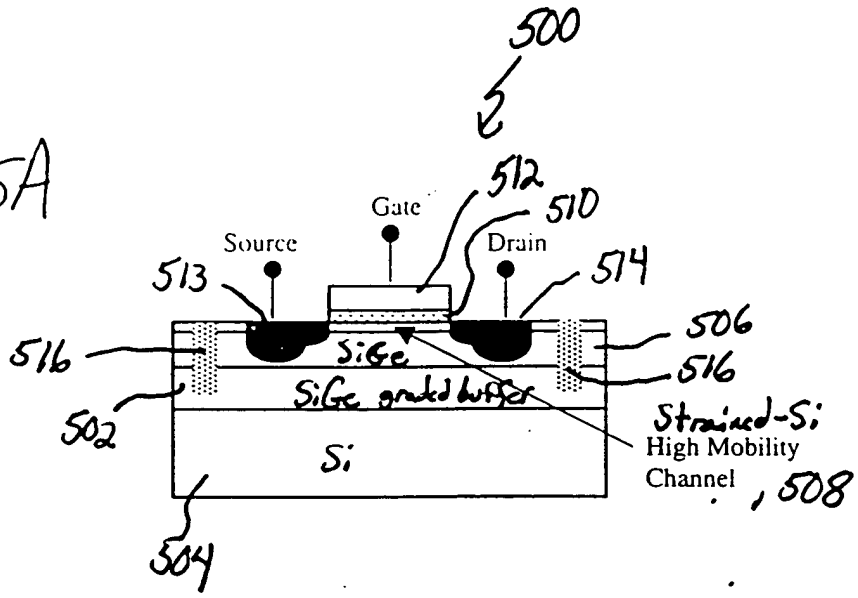
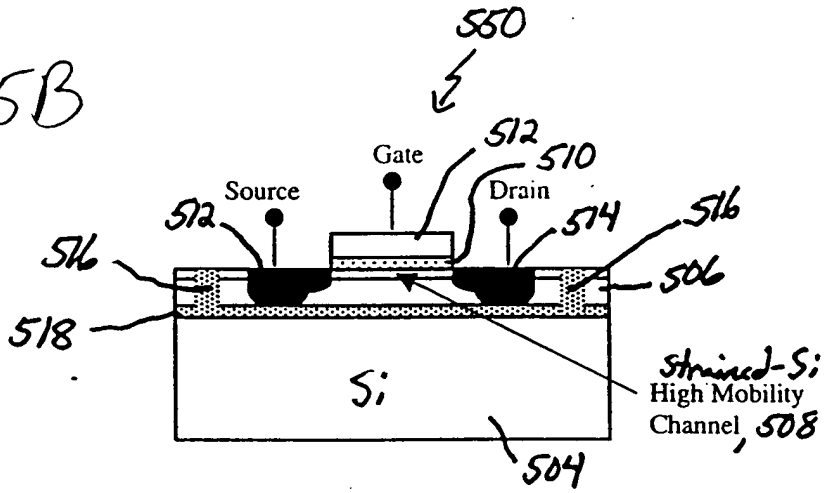

500
Gate
512
510
Source
Drain
513
514
506
516
SiGe
516
SiGe graded buffer
502
Strained-Si
High Mobility
Channel
508
Si
504

Fig. 5B


550
Gate
512
510
Source
Drain
512
514
516
516
506
518
Strained-Si
High Mobility
Channel
508
Si
504

	n enhancement	p enhancement
$Si_{0.8}Ge_{0.2}$	1.75	1
$Si_{0.7}Ge_{0.3}$	1.8	1.4

Fig. 6

	Bulk Silicon	Strained-Si on 20% SiGe: High Speed	Strained-Si on 30% SiGe: High Speed	Strained-Si on 20% SiGe: Low Power	Strained-Si on 30% SiGe: Low Power
n enhancement	1	1.75	1.8	1.75	1.8
p enhancement	1	1	1.4	1	1.4
W_p (μm)	5.4	5.4	5.4	5.4	5.4
W_n (μm)	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2
C_L (fF)	32	32	32	32	32
V_{DD} (V)	5	4.7	4.4	4.3	3.8
NM_H (V)	2.053	2.218	1.949	2.037	1.682
NM_L (V)	2.067	1.654	1.721	1.542	1.504
t_{pHL} (psec)	211.3	133.7	141.6	152.2	180.1
t_{pLH} (psec)	195.8	220.0	173.3	254.8	226.9
t_p (psec)	203.5	176.9	157.4	203.5	203.5
Power (mW)	3.93	3.93	3.93	2.87	2.21
% Speed Increase	-	**15.1%**	**29.3%**	-	-
% Power Reduction	-	-	-	**27.0%**	**43.7%**

Fig. 7

	Bulk Silicon	Strained-Si on 20% SiGe: Constant V_{DD}	Strained-Si on 30% SiGe: Constant V_{DD}	Strained-Si on 20% SiGe: High Speed Symmetrical Inverter	Strained-Si on 30% SiGe: High Speed Symmetrical Inverter	Strained-Si on 20% SiGe: Low Power Symmetrical Inverter	Strained-Si on 30% SiGe: Low Power Symmetrical Inverter
n enhancement	1	1.75	1.8	1.75	1.8	1.75	1.8
p enhancement	1	1	1.4	1	1.4	1	1.4
W_p (μm)	5.4	5.4	5.4	9.45	6.94	9.45	6.94
W_n (μm)	1.8	1.8	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2	1.2	1.2
C_L (fF)	32	32	32	32	32	32	32
V_{DD} (V)	5	5	5	4.3	4.2	3.5	3.5
NM_H (V)	2.053	2.376	2.198	1.782	1.770	1.5018	1.4796
NM_L (V)	2.067	1.751	1.923	1.794	1.781	1.5101	1.4876
t_{pHL} (psec)	211.3	120.7	117.4	152.0	149.5	204.4	204.1
t_{pLH} (psec)	195.8	195.8	139.9	145.4	143.3	202.6	202.9
t_p (psec)	203.5	158.3	128.6	148.7	146.4	203.5	203.5
Power (mW)	3.93	5.06	6.22	3.93	3.93	1.95	1.89
% Speed Increase	-	**28.6%**	**58.3%**	**36.9%**	**39.0%**	-	-
% Power Reduction	-	-	-	-	-	**50.4%**	**52.0%**

Fig. 8

Title: CMOS Inverter and Integrated Circuits Utilizing Strained Silicon Surface Channel MOSFETs
Inventor(s): Fitzgerald et al.
Atty Docket No.: ASC-043C2
Atty/Agent: Steven J. Frank/kb
Express Mail Label No. EV093437255US
Sheet 8 of 13

	Bulk Silicon	Strained-Si on 20% SiGe: High Speed	Strained-Si on 30% SiGe: High Speed	Strained-Si on 20% SiGe: Low Power	Strained-Si on 30% SiGe: Low Power
n enhancement	1	1.75	1.8	1.75	1.8
p enhancement	1	1	1.4	1	1.4
W_p (μm)	3.11	4.12	3.53	4.12	3.53
W_n (μm)	1.8	1.8	1.8	1.8	1.8
L_n, L_p (μm)	1.2	1.2	1.2	1.2	1.2
C_L (fF)	22.5	26.7	24.2	26.7	24.2
V_{DD} (V)	5	4.5	4.3	4.4	3.8
NM_H (V)	2.370	2.275	2.123	2.220	1.872
NM_L (V)	1.756	1.485	1.511	1.458	1.371
t_{pHL} (psec)	148.4	117.3	109.3	121.5	132.4
t_{pLH} (psec)	238.5	254.8	204.9	265.3	254.4
t_p (psec)	193.4	186.0	157.1	193.4	193.4
Power (mW)	2.90	2.90	2.90	2.66	1.83
% Speed Increase	-	**4.0%**	**23.1%**	-	-
% Power Reduction	-	-	-	**8.4%**	**37.1%**

Fig. 9

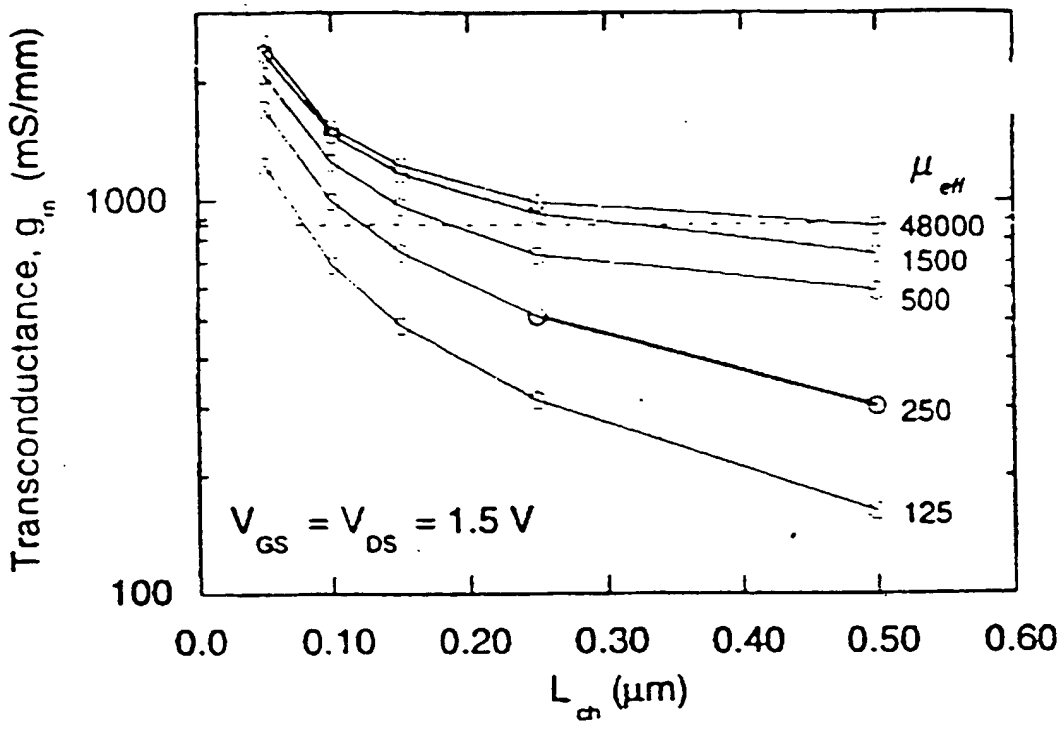

Transconductance, g_m (mS/mm)
1000
100
0.0
0.10
0.20
0.30
0.40
0.50
0.60
L_{gate} (μm)
μ_{eff}
48000
1500
500
250
125
$V_{GS} = V_{DS} = 1.5$ V

Fig. 10

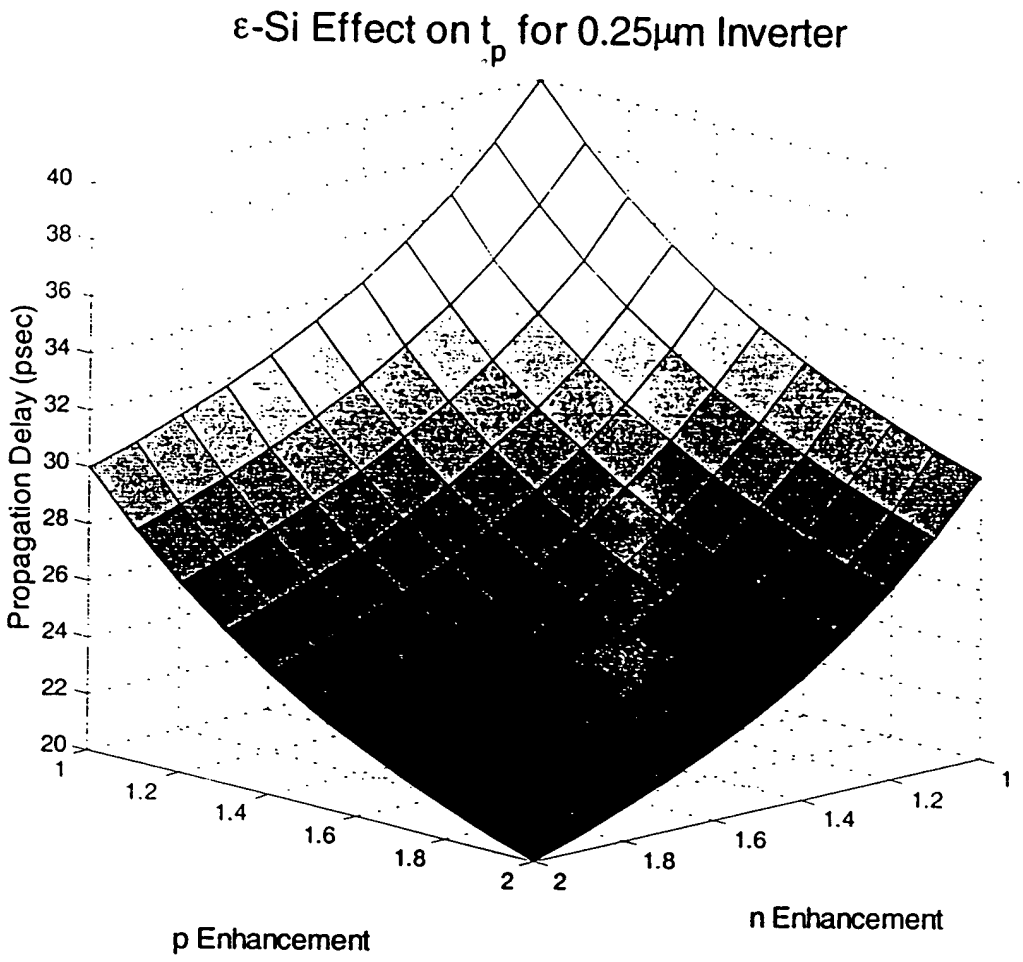

ε-Si Effect on t_p for 0.25μm Inverter
Propagation Delay (psec)
40
38
36
34
32
30
28
26
24
22
20
1
1.2
1.4
1.6
1.8
2
p Enhancement
2
1.8
1.6
1.4
1.2
1
n Enhancement

Fig. 11

Fig. 12A

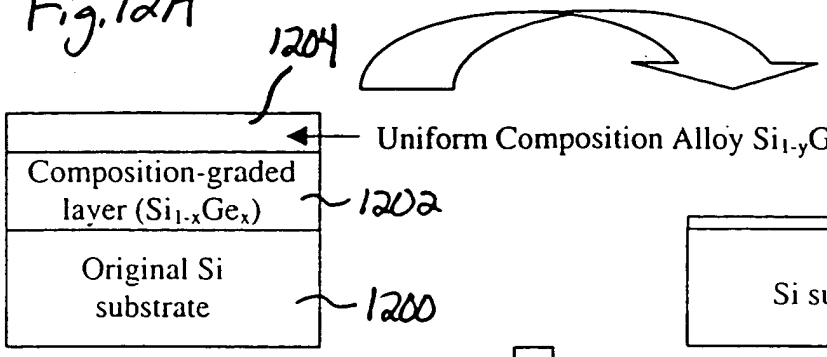


Fig. 12B

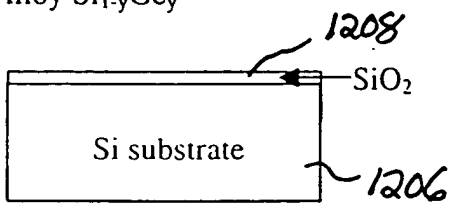


Fig. 12C

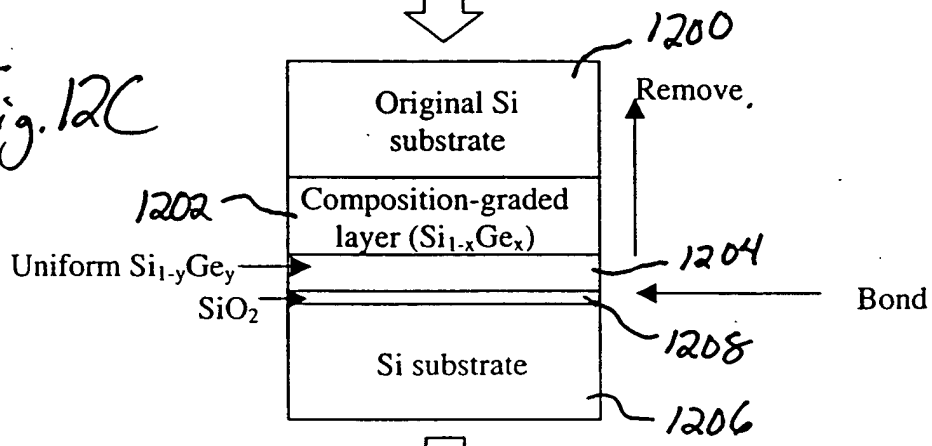


Fig. 12D

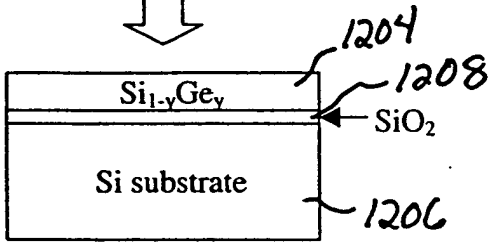
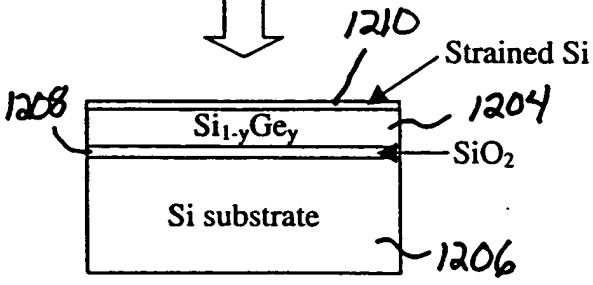


Fig. 12E



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Sheet 13 of 13

Fig. 13A

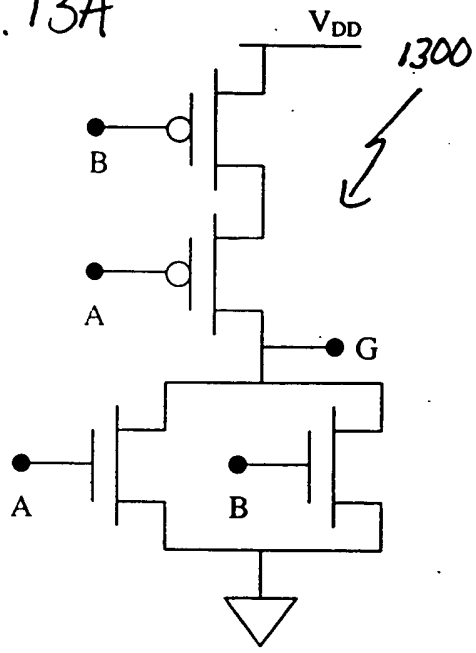

Fig. 13B

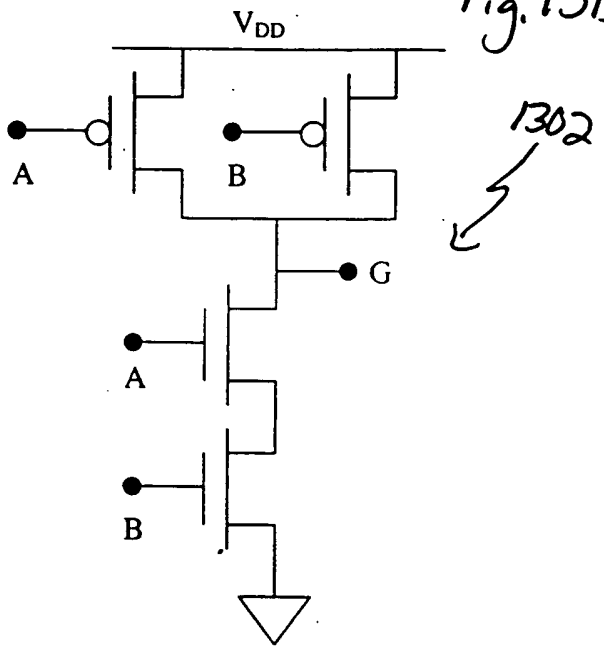

Fig. 13C